QI QI

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QUALIFICATIONS PROFILE

- Active research in read channel systems , wireless communication systems, and Ad Hoc network protocols.
- 5 years' experience in VLSI system design/verification.
- 10+ technical publications, 30+ Journal/Conference reviews, and 2 patent applications.
- Served on symposium technical program committee for IEEE WCNC2013, ICCVE2013, ICCVE2014, ICNC2014.

PROFESSIONAL EXPERIENCE

Development, design and functional verification of storage channel mixed-signal IP. Contribute to verification model development. Responsible to RTL design and development of System Verilog based verification environment and for verification closure of block/chip/system level functions for mixed signal based IP. Create comprehensive verification plan to cover all aspects of features and operations.

AVAGO TECHNOLOGIES, San Jose, CA — May 2014-Current

R&D Engineer, Staff *(May 2014-Current)*

- **Design and Verify Next Generation Read Channel.** Involved in two different product line developments. Designing and verifying next generation multi-head read channel solution. Design and verifying cryptography solution for storage products.

LSI CORPORATION, San Jose, CA — March 2011- April 2014

ASIC DvDs Engineer, Staff *(March 2013-April 2014)*

- **Design and Verify Backend Read Channel.** Involved in 2 different product line developments. Designed and verified complex interleaving network, scheduling and control circuit for iterative detector/decode, etc. Developed verification solution that significantly reduced project closure time.

ASIC DvDs Engineer, Senior *(March 2011-March 2013)*

- **Design and Verify Backend Read Channel.** Involved in 3 different product line developments. Designed and verified adaptive filter for signal interference cancellation, LDPC trapping set solution, etc.

EDUCATION

Ph.D. in Electrical Engineering (2010)
Arizona State University, Tempe, Arizona
Major Area: Algorithm-Architecture Co-Design of Signal Processing Systems

Master of Science in Electrical Engineering (2004)
Arizona State University, Tempe, Arizona
Major Area: Network Routing Protocol Design and Implementation

Bachelor of Science in Electrical Engineering (2001)
Arizona State University, Tempe, Arizona ▪ Summa Cum Laude

RESEARCH PROJECTS

Responsible for research in algorithm-architecture co-design of low complexity and high throughput wireless communication systems, including MIMO signal detectors and wireless ad hoc protocols.

- Design Sphere Decoder for Multiprocessor Architectures.
- Design Fixed-point FFT for SODA Architectures.
- Design Battery Aware Ad Hoc routing Protocols.
- Design Geographic Defined Hierarchical Routing Algorithm.

PATENTS

- "Systems and Methods for Trapping Set Disruption," US Patent, application pending (13/770,030), filed February 2013.
- "Modified Targeted Symbol Flipping for Non-binary LDPC Codes," US Patent, application pending (13/629,726), filed September 2012.

PUBLICATIONS

- Lei Zhang, Cihang Xie, Tao Jiang, Junyang Shen, Qi Qi and Dexiang Meng. Prediction-based MAC-Layer Sensing in Cognitive Radio Networks. Wiley of Wireless Communications and Mobile Computing, doi: 10.1002/wcm.2498.
- Liang Yu, Tao Jiang, Yang Cao, and Qi Qi. Joint Workload and Battery Scheduling with Heterogeneous Service Delay Guarantees for Data Center Energy Cost Minimization. IEEE Transactions on Parallel and Distributed Systems, doi: 10.1109/TPDS.2014.2329491.
- Liang Yu, Tao Jiang, Yang Cao, and Qi Qi. Carbon-aware Energy Cost Minimization for Distributed Internet Data Centers in Smart Microgrids. IEEE Internet of Things Journal, vol. 1, issue 3, pp. 255-264, June 2014.
- Tao Jiang, Chunxing Ni, Chang Xu, and Qi Qi. Curve Fitting Based Tone Reservation Method with Low Complexity for PAPR Reduction in OFDM Systems. IEEE Communications Letter, vol. 18, issue 5, pp. 805-808, May 2014.
- Chen Ye, Zijun Li, Tao Jiang, Chunxing Ni, and Qi Qi. PAPR Reduction of OQAM-OFDM Signals Using Segmental PTS Scheme with Low Complexity. IEEE Transactions on Broadcasting, vol. 60, no. 1, pp. 141-147, Mar. 2014.
- Xianfeng Deng, Tao Jiang, Yang Zhou, Chen Ye, and Qi Qi. PAPR reduction in SFBC MIMO-OFDM Systems by Tone Reservation. International Journal of Communication Systems, DOI: 10.1002/dac.2582, Jun. 2013.
- Qi Qi and Chaitali Chakrabarti, Parallel Soft-Output Sphere Decoding with Fixed Complexity. Journal of Signal Processing Systems, vol. 68 Issue 2, August. 2012.
- Qi Qi and Chaitali Chakrabarti, Parallel Soft-Output Sphere Decoder. Proc. Of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Oct. 2010.
- Qi Qi and Chaitali Chakrabarti, Sphere Decoding for Multiprocessor Architectures. Proc. Of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Oct. 2007.
- Qi Qi and Chaitali Chakrabarti, Battery Aware Wireless Ad-Hoc Routing Protocol. Proc. of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Nov. 2005.

PROFESSIONAL ACTIVITIES

- Invited reviewer for IEEE Wireless Communications and Networking Conference 2013
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2013
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2014
- Invited reviewer for IEEE International Conference on Computing, Networking and Communications 2014
- Invited reviewer for IEEE Globalcom Signal Processing for Communications Symposium 2013
- Invited reviewer for IEEE Globalcom Signal Processing for Communications Symposium 2014
- Invited reviewer for IEEE Globalcom Symposium on Selected Area in Communications 2014
- Invited reviewer for IEEE Transactions on Wireless Communications 2014.
- Invited reviewer for IEEE Transactions on Vehicular Technology 2014.
- Invited reviewer for KSII Transactions on Internet and Information Systems 2014.
- Invited reviewer for Security and Communication Networks 2014.
- Invited reviewer for International Journal of Communication Systems 2014.