QI QI

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INTERESTS: Algorithm-architecture co-design of VLSI systems for storage and communication systems.

QUALIFICATIONS PROFILE

- Active research in read channel system, wireless communication systems, and Ad Hoc network protocols.
- 6 years of experience in VLSI system design/verification.
- 10 technical publications, 80+ Journal/Conference reviews, and 2 patents.
- Served on symposium technical program committee for IEEE WCNC2013, ICCVE2013, GC2013SPC, ICCVE2014, ICNC2014, GC2014SPC, CHINACOM2015, AR4MET2015, ICCME2015, ICCVE2015, GC2015SAC, ICC2016SAC and ICCVE2016.

PROFESSIONAL EXPERIENCE

Development, design and functional verification of storage channel DSP IPs. Contribute to verification model development. Responsible to RTL design and development of System Verilog based verification environment and for verification closure of block/chip/system level IP functions.

BROADCOM LIMITED (FORMER AVAGO TECHNOLOGIES), San Jose, CA **May 2014-Current**

R&D Engineer, IC Design 4 *(May 2014-Current)*
Projects

- **Backend Read Channel Emulation Environment Development (FPGA).** Involved in firmware development and emulation of backend solution for storage products.
- **Design and Verify Frontend Read Channel (DSP).** Involved in 2 multi-head read channel product line developments. Designing and verifying next generation multi-head read channel solution.

LSI CORPORATION, San Jose, CA **March 2011- April 2014**

ASIC DvDs Engineer, Staff *(March 2013-April 2014)*
Projects

- **Design and Verify Backend Read Channel (ECC).** Involved in 2 different product line developments. Designed and verified complex interleaving networks, scheduling and control circuit for iterative detector/decoder, etc. Developed verification solution that significantly reduced project closure time.

ASIC DvDs Engineer, Senior *(March 2011-March 2013)*
Projects

- **Design and Verify Backend Read Channel (ECC).** Involved in 3 different product line developments. Designed and verified adaptive filter for signal interference cancellation, LDPC trapping set solution, etc.

EDUCATION

Ph.D. in Electrical Engineering (2010)
Arizona State University, Tempe, Arizona
Major Area: Algorithm-Architecture Co-Design of Signal Processing Systems

Master of Science in Electrical Engineering (2004)
Arizona State University, Tempe, Arizona

Major Area: Network Routing Protocol Design and Implementation

Bachelor of Science in Electrical Engineering (2001)
Arizona State University, Tempe, Arizona ▪ Summa Cum Laude

PATENTS

- "Modified Targeted Symbol Flipping for Non-binary LDPC Codes," US Patent number 8977926, March 2015.
- "Systems and Methods for Trapping Set Disruption," US Patent number 8949696, Feb. 2015.

PUBLICATIONS

- Liang Yu, Tao Jiang, Yang Cao, and Qi Qi. Joint Workload and Battery Scheduling with Heterogeneous Service Delay Guarantees for Data Center Energy Cost Minimization. IEEE Transactions on Parallel and Distributed Systems, vol. 26, issue 7, pp. 1937-1947, July 2015.
- Lei Zhang, Cihang Xie, Tao Jiang, Junyang Shen, Qi Qi and Dexiang Meng. Prediction-based MAC-Layer Sensing in Cognitive Radio Networks. Wiley of Wireless Communications and Mobile Computing, DOI: 10.1002/wcm.2498, July 2014.
- Liang Yu, Tao Jiang, Yang Cao, and Qi Qi. Carbon-aware Energy Cost Minimization for Distributed Internet Data Centers in Smart Microgrids. IEEE Internet of Things Journal, vol. 1, issue 3, June 2014.
- Tao Jiang, Chunxing Ni, Chang Xu, and Qi Qi. Curve Fitting Based Tone Reservation Method with Low Complexity for PAPR Reduction in OFDM Systems. IEEE Communications Letter, vol. 18, issue 5, pp. 805-808, May 2014.
- Chen Ye, Zijun Li, Tao Jiang, Chunxing Ni, and Qi Qi. PAPR Reduction of OQAM-OFDM Signals Using Segmental PTS Scheme with Low Complexity. IEEE Transactions on Broadcasting, vol. 60, no. 1, pp. 141-147, Mar. 2014.
- Xianfeng Deng, Tao Jiang, Yang Zhou, Chen Ye, and Qi Qi. PAPR reduction in SFBC MIMO-OFDM Systems by Tone Reservation. International Journal of Communication Systems, DOI: 10.1002/dac.2582, Jun. 2013.
- Qi Qi and Chaitali Chakrabarti, Parallel Soft-Output Sphere Decoding with Fixed Complexity. Journal of Signal Processing Systems, vol. 68 Issue 2, August. 2012.
- Qi Qi and Chaitali Chakrabarti, Parallel Soft-Output Sphere Decoder. Proc. Of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Oct. 2010.
- Qi Qi and Chaitali Chakrabarti, Sphere Decoding for Multiprocessor Architectures. Proc. Of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Oct. 2007.
- Qi Qi and Chaitali Chakrabarti, Battery Aware Wireless Ad-Hoc Routing Protocol. Proc. of the IEEE Workshop on Design and Implementation of Signal Processing Systems, Nov. 2005.

PROFESSIONAL ACTIVITIES

- Serving as IEEE Data Storage Technical Committee Treasurer in 2016
- Invited reviewer for IEEE ICC SAC Data Storage 2016
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2016
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2015
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2014
- Invited reviewer for IEEE International Conference on Connected Vehicles and Expo 2013
- Invited reviewer for IEEE International Conference on Computing, Networking and Communications 2014
- Invited reviewer for IEEE Globalcom Signal Processing for Communications Symposium 2014
- Invited reviewer for IEEE Globalcom Signal Processing for Communications Symposium 2013
- Invited reviewer for IEEE Globalcom Symposium on Selected Area in Communications 2014
- Invited reviewer for IEEE Transactions on Wireless Communications 2014
- Invited reviewer for IEEE Transactions on Vehicular Technology 2014.
- Invited reviewer for KSII Transactions on Internet and Information Systems 2014
- Invited reviewer for Security and Communication Networks 2014
- Invited reviewer for International Journal of Communication Systems 2014
- Invited reviewer for IEEE Wireless Communications and Networking Conference 2013