XINMIAO ZHANG

Dept. of Electrical & Computer Engineering
The Ohio State University
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EDUCATION

Ph. D. in Electrical Engineering — Jun. 2005
University of Minnesota, Twin Cities, MN

M. S. in Electrical Engineering — May 2000
Tianjin University, Tianjin, China

B. E. in Electrical Engineering — Jun. 1997
Tianjin University, Tianjin, China

PROFESSIONAL EXPERIENCES

Tenured Associate Professor — Aug. 2017- present
Department of Electrical and Computer Engineering
The Ohio State University, Columbus, OH

Senior Technologist (Senior Principal) — Jun. 2016-Aug. 2017
Western Digital Corporation (acquired SanDisk), San Jose, CA

Principal Research Engineer — Jul. 2013-May. 2016
SanDisk Corporation, San Jose, CA

Tenured Associate Professor — Jul. 2010-Jun. 2013
Department of Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, OH

Visiting Professor — Jul. 2011-Jun. 2013
Department of Electrical Engineering
University of Washington, Seattle, WA

Timothy E. and Allison L. Schroeder Professor — Mar. 2006- Jun. 2013
Department of Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, OH

Assistant Professor — Aug. 2005-Jun. 2010
Department of Electrical Engineering and Computer Science
Case Western Reserve University, Cleveland, OH

Visiting Professor — May 2008-Aug. 2008
Qualcomm, San Diego, CA

RESEARCH INTERESTS

Digital storage and communications, security, VLSI architecture design, and signal processing

HONORS & AWARDS

- *Best Paper Award* at International SanDisk Technology Conference, 2016
- *Best Associate Editor* for IEEE Trans. on Circuits and Systems-I, 2013
- Nominee for *IEEE Very Large Scale Integration Systems Best Paper Award*, 2012
- *Faculty Research Award*, Department of Electrical Engineering and Computer Science, Case Western Reserve University, 2010
- National Science Foundation (NSF) *Faculty Early Career Development (CAREER) Award*, Jan. 2009
- Nominee for *Carl F. Wittke Award for Excellence in Undergraduate Teaching*, Case Western Reserve University, 2008
- *Best Paper Award* at the ACM Great Lakes Symposium on VLSI 2004. The paper became one of the top ten downloads from the ACM digital library in Jan. 2005
- *First Place in Student Paper Contest* at the Asilomar Conference on Signals, Systems and Computers, 2004

PROFESSIONAL AFFILIATIONS & ACTIVITIES

Editorship

- Associate editor, *IEEE Open Journal of Circuits and Systems*, 2019-present
- Guest editor, *IEEE Open Journal of Circuits and Systems Special Section*, 2020
- Guest editor, *Springer Journal of Signal Processing Systems Special Section*, 2020
- Associate editor, *IEEE Transactions on Circuits and Systems-I*, 2010-2019
- Associate editor, *International Journal of Circuits, Systems and Computers*, 2009-2010
- Co-editor, *Wireless Security and Cryptography: Specifications and Implementations*, CRC Press, 2007
- Guest editor, *Special Issue on Next Generation Hardware Architectures for Secure Mobile Computing*, *Mobile Networks and Applications (MONET) Journal*, Springer-Verlag, 2007

Technical & Services Committees

- Member, Board of Governors, IEEE Circuits and Systems Society, 2019-2121.
- Vice-Chair from Academia, Data Storage Technical Committee, IEEE Communications Society, 2019-2020
- Vice-Chair from Industry, Data Storage Technical Committee, IEEE Communications Society, 2017-2018

- Member, Industry Technical Working Group, IEEE Signal Processing Society, 2020-present
- Member, Circuits and Systems for Communications (CASCOM) Technical Committee, IEEE Circuits and Systems Society, 2007-present
- Member, VLSI Systems and Applications (CASVSA) Technical Committee, IEEE Circuits and Systems Society, 2006-present
- Chair, Seasonal Schools in Signal Processing Program, IEEE Signal Processing Society, 2013-2015
- Member, Membership Services Committee, IEEE Signal Processing Society, 2010-2015
- Member, Design and Implementation of Signal Processing Systems (DISPS) Technical Committee, IEEE Signal Processing Society, 2008-2014

Conference Committees

- WiCAS Co-Chair, IEEE International Symposium on Circuits and Systems (ISCAS) 2021
- Reviewer committee member, IEEE International Symposium on Circuits and Systems (ISCAS) 2007-2021
- Technical program committee member, IEEE International Conference on Communications (ICC) 2014-15, 2018, 2020-21
- Technical program committee member, IEEE Workshop on Signal Processing Systems (SiPS) 2008-2020
- Technical program committee member, IEEE Global Communications Conference (GLOBECOM) 2009, 2016-2020
- Technical program committee member, Non-Volatile Memories Workshop 2011-2014, 2016-2021
- Technical Program Chair, IEEE Workshop on Signal Processing Systems (SiPS) 2019
- Chair, Data Storage Track, IEEE International Conference on Communications (ICC) 2019
- Tutorial Co-Chair, IEEE Workshop on Signal Processing Systems (SiPS) 2018
- Co-Chair, Late Breaking News (LBN) Track, IEEE International Symposium on Circuits and Systems (ISCAS) 2018
- Industrial Committee member, IEEE International Symposium on Circuits and Systems (ISCAS) 2018
- Special session co-organizer, IEEE International Symposium on Circuits and Systems (ISCAS) 2018
- Member, Student Paper Contest Panel, IEEE International Symposium on Circuits and Systems (ISCAS) 2018

- Industry Liaison Co-Chair, IEEE Workshop on Signal Processing Systems (SiPS) 2017
- Publication Chair, IEEE International System-on-Chip Conference (SOCC), 2016
- Co-Chair, International SanDisk Technology Conference, Enterprise Storage Track, 2016.
- Technical program committee member, IEEE Global Conference on Signal and Information Processing (GlobalSIP) 2014, 2015
- Publication Chair, IEEE Workshop on Signal Processing Systems (SiPS) 2012
- Technical program committee member, ACM Great Lakes Symposium on VLSI (GLSVLSI) 2006, 2012
- Student Paper Contest Chair, Asilomar Conference on Signals, Systems, and Computers 2010
- Publication Chair, ACM Great Lakes Symposium on VLSI (GLSVLSI) 2007, 2008

PUBLICATIONS

Books

1. X. Zhang, *VLSI Architectures for Modern Error-Correcting Codes*, CRC Press, 2015.
2. N. Sklavos and X. Zhang Ed. *Wireless Security and Cryptography: Specifications and Implementations*, CRC Press, 2007.

Book Chapter

1. X. Zhang, "Efficient VLSI architectures for the AES algorithm" in N. Sklavos and X. Zhang Ed., *Wireless Security and Cryptography: Specifications and Implementations*, CRC press, 2007.

Journal Papers

1. Z. Xie and X. Zhang, "Fast nested key equation solvers for generalized integrated interleaved decoder," *IEEE Trans. Circuits and Syst.-I*, 2020.
2. X. Zhang, "VLSI architectures for Reed-Solomon codes: classic, nested, coupled, and beyond," *IEEE Open Journal of Circuits and Syst.*, pp. 157-169, 2020.
3. Z. Xie and X. Zhang, "Reduced-complexity key equation solvers for generalized integrated interleaved BCH decoders," *IEEE Trans. Circuits and Syst.-I*, 2020.
4. Z. Xie and X. Zhang, "Scaled nested key equation solver for generalized integrated interleaved decoder," *IEEE Trans. Circuits and Syst.-II*, vol. 67, no. 11, pp. 2457-2461, 2020.
5. X. Zhang and Z. Xie, "Efficient VLSI architectures for coupled-layered regenerating codes," *IEEE Trans. Circuits and Syst.-II*, vol. 67, no. 10, pp. 1869-1873, Oct. 2020.
6. Zhang and Z. Xie, "Relaxing the constraints on locally recoverable erasure codes by finite field element variation," *IEEE Communications Letters*, vol. 23, no. 10, pp. 1680-1683, Oct. 2019.

7. X. Zhang and Z. Xie, "Efficient architectures for generalized integrated interleaved decoder," *IEEE Trans. on Circuits and Systems-I*, vol. 66, no. 10, pp. 4018-4031, Oct. 2019.
8. X. Zhang and Y. Lao, "On the construction of composite finite field for hardware obfuscation," *IEEE Trans. on Computers*, vol. 68, no. 9, pp. 1353-1364, 2019.
9. X. Zhang, "A low-power parallel architecture for linear feedback shift registers," *IEEE Trans. on Circuits and Systems-II*, vol. 66, no. 3, pp. 412-416, Mar. 2019.
10. X. Zhang, "Generalized three-layer integrated interleaved codes," *IEEE Communications Letters,* vol. 22, no. 3, pp. 442-445, Mar. 2018.
11. X. Zhang, "Modified generalized integrated interleaved codes for local erasure recovery," *IEEE Communications Letters,* vol. 21, no. 6, pp 1241-1244, Jun. 2017.
12. X. Zhang and Y. Tai, "Low-complexity transformed encoder architectures for quasi-cyclic non-binary LDPC codes over subfields," *IEEE Trans. on VLSI Systems*, vol. 25, no. 4, pp. 1342-1351, Apr. 2017.
13. X. Zhang, S. Sprouse and I. Ilani, "A flexible and low-complexity local erasure recovery scheme," *IEEE Communications Letters,* vol. 50, no. 11, pp. 2129 - 2132, Nov. 2016.
14. X. Zhang, "Low-complexity Min-max non-binary LDPC decoders," *Journal of Communications,* vol. 10, no. 11, pp. 836-842, Nov. 2015.
15. F. Cai, X. Zhang, D. Declercq, S. K. Planjery and B. Vasic, "Finite alphabet iterative decoders for LDPC codes: optimization, architecture and analysis," *IEEE Trans. on Circuits and Systems-I*, vol. 61, no. 5, pp. 1366-1375, May 2014.
16. F. Cai and X. Zhang, "Relaxed min-max decoder architectures for non-binary LDPC code," *IEEE Trans. on VLSI Systems,* vol. 21, no. 11, pp. 2010-2023, Nov. 2013.
17. F. Cai and X. Zhang, "Efficient check node processing architectures for non-binary LDPC decoding using power representation," *Springer Journal of Signal Processing Systems*, vol. 76, no. 2, pp. 211-222, Nov. 2013.
18. X. Zhang, "An efficient interpolation-based Chase BCH decoder," *IEEE Trans. on Circuits and Systems-II*, vol. 60, no. 4, pp. 212-216, Apr. 2013.
19. X. Zhang and Y. Zheng, "Generalized backward interpolation for algebraic soft-decision decoding of Reed-Solomon codes," *IEEE Trans. on Communications,* vol. 61, no. 1, pp. 13-23, Jan. 2013.
20. X. Zhang, F. Cai, and S. Lin, "Low-complexity reliability-based message-passing decoder architectures for non-binary LDPC codes," *IEEE Trans. on VLSI Systems,* vol. 20, no. 11, pp. 1938-1950. Nov. 2012.
21. X. Zhang and Z. Wang, "A low-complexity three-error-correcting BCH decoder for optical transport network," *IEEE Trans. on Circuits and Systems-II*, vol. 59, no. 10, pp. 663-667, Oct. 2012.
22. X. Zhang, Y. Wu, J. Zhu, and Y. Zheng, "Novel polynomial selection and interpolation for low-complexity Chase algebraic soft-decision Reed-Solomon decoding," *IEEE Trans. on VLSI Systems,* vol. 20, no. 7, pp. 1318-1322, Jul. 2012.

23. X. Zhang and Y. Zheng, "Systematically re-encoded algebraic soft-decision Reed-Solomon decoder," *IEEE Trans. on Circuits and Systems-II*, vol. 59, no. 6, pp. 376-380, Jun. 2012.
24. X. Zhang, J. Zhu and W. Zhang, "Efficient re-encoder architectures for algebraic soft-decision Reed-Solomon decoding," *IEEE Trans. on Circuits and Systems-II*, vol. 59, no. 3, pp. 163-167, Mar. 2012.
25. J. Zhu and X. Zhang, "Efficient generalized minimum-distance decoders of Reed-Solomon codes," *Springer Journal of Signal Processing Systems*, vol. 66, no. 3, pp. 245-257, Mar. 2012.
26. X. Zhang, J. Zhu and W. Zhang, "Modified low-complexity Chase soft-decision decoder of Reed-Solomon codes," *Springer Journal of Signal Processing Systems*, vol. 66, no. 1, pp. 3-13, Jan. 2012.
27. X. Zhang and F. Cai, "Reduced-complexity decoder architecture for non-binary LDPC codes," *IEEE Trans. on VLSI Systems*, vol. 19, no. 7, pp. 1229-1238, Jul. 2011.
28. X. Zhang and F. Cai, "Efficient partial-parallel decoder architecture for quasi-cyclic non-binary LDPC codes," *IEEE Trans. on Circuits and Systems-I,* vol. 58, no. 2, pp. 402-414, Feb. 2011.
29. S. Paul, F. Cai, X. Zhang and S. Bhunia, "Reliability-driven ECC allocation for multiple bit error resilience in processor cache," *IEEE Trans. on Computers,* vol. 60, no. 1, pp. 20-34, Jan. 2011.
30. X. Zhang and J. Zhu, "Algebraic soft-decision decoder architectures for long Reed-Solomon codes," *IEEE Trans. on Circuits and Systems-II,* vol. 57, no. 10, pp. 787-792, Oct. 2010.
31. X. Zhang and J. Zhu, "High-throughput interpolation architecture for algebraic soft-decision Reed-Solomon decoding," *IEEE Trans. on Circuits and Systems-I*, vol. 57, no. 3, pp. 581-591, Mar. 2010.
32. J. Zhu, X. Zhang and Z. Wang, "Backward interpolation for algebraic soft-decision Reed-Solomon decoding," *IEEE Trans. on VLSI Systems*, vol. 17, no. 11, pp. 1602-1615, Nov. 2009.
33. J. Zhu and X. Zhang, "Efficient VLSI architecture for soft-decision decoding of Reed-Solomon codes," *IEEE Trans. on Circuits and Systems-I*, vol. 55, no. 10, pp. 3050-3062, Nov. 2008.
34. X. Zhang, "Further exploring the strength of prediction in the factorization of soft-decision Reed-Solomon decoding," *IEEE Trans. on VLSI Systems*, vol. 15, no. 7, pp. 811-820, Jul. 2007.
35. X. Zhang, "Reduced complexity interpolation architecture for soft-decision Reed-Solomon decoding," *IEEE Trans. on VLSI Systems,* vol. 14, no. 10, pp. 1156-1161, Oct. 2006.
36. X. Zhang and K. K. Parhi, "On the optimum constructions of composite field for the AES algorithm," *IEEE Trans. on Circuits and Systems-II*, vol. 53, no. 10, pp. 1153-1157, Oct. 2006.

37. X. Zhang and K. K. Parhi, "High-speed architectures for parallel long BCH encoders," *IEEE Trans. on VLSI Systems,* vol. 13, no. 7, pp. 872-877, Jul. 2005.
38. X. Zhang and K. K. Parhi, "Fast factorization architecture in soft-decision Reed-Solomon decoding," *IEEE Trans. on VLSI Systems*, vol. 13, no. 4, pp. 413-426, Apr. 2005.
39. X. Zhang and K. K. Parhi, "High-speed VLSI architectures for the AES algorithm," *IEEE Trans. on VLSI Systems*, vol. 12, no. 9, pp. 957-967, Sep. 2004.
40. X. Zhang and K. K. Parhi, "Implementation approaches for the Advanced Encryption Standard algorithm," *IEEE Circuits and Systems Magazine*, vol. 2, no. 4, pp. 24-46, Fourth Quarter 2002.

Peer-reviewed Conference Papers

1. Y. J. Tang and X. Zhang, "Low-complexity architectures for parallel long BCH encoders," *Proc. of IEEE Workshop on Signal Processing Systems*, Coimbra, Portugal, Oct. 2020.
2. X. Zhang, "High-speed and low-complexity parallel long BCH encoder," *Proc. of IEEE International Symposium on Circuits and Systems*, Seville, Spain, May 2020.
3. J. Zhou and X. Zhang, "A new logic-locking scheme resilient to gate removal attack," *Proc. of IEEE International Symposium on Circuits and Systems*, Seville, Spain, May 2020.
4. P. Shvartsman and X. Zhang, "Side channel attack resistant AES design based on finite field construction variation," *Proc. of IEEE Workshop on Signal Processing Systems*, Nanjing, China, Oct. 2019.
5. X. Zhang, "Decoding of generalized three-layer integrated interleaved codes," *Proc. of IEEE International Symposium on Information Theory*, Paris, France, Jul. 2019.
6. X. Zhang and Y. J. Tang, "Reducing parallel linear feedback shift register complexity through input tap modification," *Proc. of IEEE International Symposium on Circuits and Systems*, Sapporo, Japan, May 2019.
7. X. Zhang, P. Shvartsman, J. Zhou, and E. Y. Tawfik, "Hardware obfuscation of AES through finite field construction variation," *Proc. of IEEE International Symposium on Circuits and Systems*, Sapporo, Japan, May 2019.
8. A. Sharma, X. Zhang, and Y. Lao, "Hardware obfuscation through reconfigurable finite field arithmetic units," *Proc. of IEEE International Symposium on Circuits and Systems*, Sapporo, Japan, May 2019.
9. X. Zhang, "Systematic encoder of generalized three-layer integrated interleaved codes," *Proc. of IEEE International Conference on Communications*, Shanghai, China, May 2019.
10. X. Zhang and M. O'Sullivan, "Ultra-compressed three-error-correcting BCH decoder," *Proc. of IEEE International Symposium on Circuits and Systems*, Florence, Italy, May 2018.

11. X. Zhang and A. Bazarsky, "Perfect column-layered two-bit message-passing LDPC decoder and architectures," *Proc. of IEEE International Symposium on Circuits and Systems*, Florence, Italy, May 2018.
12. X. Zhang, I. Dror, and S. Alterman, "Low-power partial-parallel Chien search architecture with polynomial degree reduction," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 2459-2462, Montreal, Canada, May 2016.
13. X. Zhang, "Modified trellis-based Min-max decoder for non-binary LDPC codes," *Proc. of International Conference on Computing, Networking and Communications*, pp. 613-617, Anaheim, CA, Feb. 2015.
14. X. Zhang and Y. Tai, "High-speed multi-block-row layered decoding for quasi-cyclic LDPC codes," *Proc. of IEEE Global Conference on Signal and Information Processing*, pp. 11-14, Atlanta, GA, Dec. 2014.
15. X. Zhang, F. Cai, and M. P. Anantram, "Low-energy and low-latency error correction for phase change memory," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 1236-1239, Beijing, China, May 2013.
16. F. Cai, X. Zhang, D. Declercq, B. Vasic, D. V. Nguyen, and S. K. Planjery, "Low-complexity finite alphabet iterative decoders for LDPC codes," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 1332-1335, Beijing, China, May 2013.
17. W. Zhang, J. Wang, and X. Zhang, "Low-power design of Reed-Solomon encoders," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 1560-1563, Beijing, China, May 2013.
18. W. Zhang, X. Zhang and H. Wang, "Increasing the energy efficiency of WSNs using algebraic soft-decision Reed-Solomon decoders," *Proc. of IEEE Asia Pacific Conference on Circuits and Systems*, pp. 49-52, Taiwan, Dec. 2012.
19. F. Cai and X. Zhang, "Efficient check node processing architecture for non-binary LDPC decoding using power representation," *Proc. of IEEE Workshop on Signal Processing Systems,* pp. 137-142, Quebec City, Canada, Oct. 2012.
20. X. Zhang, F. Cai and R. Shi, "Low-power LDPC decoding based on iteration prediction," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 3041-3044, Seoul, Korea, May 2012.
21. X. Zhang, Y. Zheng, and Y. Wu, "A Chase-type Koetter-Vardy algorithm for soft-decision Reed-Solomon decoding," *Proc. of International Conference on Computing, Networking and Communications*, pp. 466-470, Maui, HI, Feb. 2012.
22. X. Zhang and F. Cai, "An efficient architecture for iterative soft reliability-based majority-logic non-binary LDPC decoding," *Proc. of Asilomar Conference on Signals, Systems, and Computers*, pp. 885-888, Pacific Grove, CA, Nov. 2011.
23. X. Zhang, J. Zhu and Y. Wu, "Efficient one-pass Chase soft-decision BCH decoder for multi-level cell NAND flash memory," *Proc. of IEEE International Midwest Symposium on Circuits and Systems*, Seoul, Korea, Aug. 2011.

24. X. Zhang, and F. Cai, "Reduced-memory forward-backward check node processing architecture for non-binary LDPC decoding," *Proc. of IEEE International Midwest Symposium on Circuits and Systems*, Seoul, Korea, Aug. 2011.
25. X. Zhang, Y. Wu and J. Zhu, "A novel polynomial selection scheme for low-complexity Chase algebraic soft-decision Reed-Solomon decoding," *Proc. of IEEE International Symposium on Circuits and Systems,* pp. 2689-2692, Rio De Janeiro, Brazil, May 2011.
26. X. Zhang and F. Cai, "Low-complexity architectures for reliability-based message-passing non-binary LDPC decoding," *Proc. of IEEE International Symposium on Circuits and Systems,* pp. 1303-1306, Rio De Janeiro, Brazil, May 2011.
27. X. Zhang and F. Cai, "Reduced-latency scheduling scheme for the Min-max non-binary LDPC decoding," *Proc. of IEEE Asia Pacific Conference on Circuits and Systems*, pp. 414-417, Kuala Lumpur, Malaysia, Dec. 2010.
28. X. Zhang and J. Zhu, "Reduced-complexity multi-interpolator algebraic soft-decision Reed-Solomon decoder," *Proc. of IEEE Workshop on Signal Processing Systems,* pp. 398-403, San Francisco, CA, Oct. 2010.
29. X. Zhang and F. Cai, "Reduced-complexity check node processing for non-binary LDPC decoding," *Proc. of IEEE Workshop on Signal Processing Systems,* pp. 70-75, San Francisco, CA, Oct. 2010.
30. X. Zhang and F. Cai, "Reduced-complexity extended Min-sum check node processing for non-binary LDPC decoding," *Proc. of IEEE International Midwest Symposium on Circuits and Systems*, pp. 737-740, Seattle, WA, Aug. 2010.
31. J. Zhu and X. Zhang, "High-speed re-encoder design for algebraic soft-decision Reed-Solomon decoding," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 465-468, Paris, France, May 2010.
32. X. Zhang and F. Cai, "Partial-parallel decoder architecture for quasi-cyclic non-binary LDPC codes," *Proc. of IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 1506-1509, Dallas, TX, Mar. 2010.
33. J. Zhu and X. Zhang, "Efficient generalized minimum-distance decoder of Reed-Solomon codes," *Proc. of IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 1502-1505, Dallas, TX, Mar. 2010.
34. Y. Chen and X. Zhang, "High-speed architecture for image reconstruction based on compressive sensing," *Proc. of IEEE International Conference on Acoustics, Speech and Signal Processing*, pp. 1574-1577, Dallas, TX, Mar. 2010.
35. X. Zhang and J. Zhu, "Interpolation-based hard-decision Reed-Solomon decoders," *Proc. of International Symposium on Integrated Circuits*, pp. 175-178, Singapore, Dec. 2009.
36. J. Zhu and X. Zhang, "Factorization-free low-complexity Chase soft-decision decoding of Reed-Solomon codes," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 2677-2680, Taiwan, May 2009.

37. X. Zhang, "VLSI architecture design for algebraic soft-decision Reed-Solomon decoding," *Proc. of Asilomar Conference on Signals, Systems, and Computers*, pp. 1518-1522, Pacific Grove, CA, Nov. 2008.
38. J. Zhu and X. Zhang, "Scalable interpolation architecture for soft-decision Reed-Solomon decoding," *Proc. of IEEE Asia Pacific Conference on Circuits and Systems*, pp. 41-44, Macao, China, Nov. 2008.
39. Z. Cui, Z. Wang, X. Zhang and Q. Jia, "Efficient decoder design for high-throughput LDPC decoding," *Proc. of IEEE Asia Pacific Conference on Circuits and Systems*, pp. 1640-1643, Macao, China, Nov. 2008.
40. Q. Li, Z. Wang, X. Zhang and X. Liu, "Efficient architecture for the Tate pairing in characteristic three," *Proc. of IEEE Asia Pacific Conference on Circuits and Systems*, pp. 1111-1115, Macao, China, Nov. 2008.
41. J. Zhu, X. Zhang and Z. Wang, "Combined interpolation architecture for soft-decision decoding of Reed-Solomon codes," *Proc. of IEEE International Conference on Computer Design*, pp. 526-531, Lake Tahoe, CA, Oct. 2008.
42. X. Zhang and J. Zhu, "Efficient interpolation architecture for soft-decision Reed-Solomon decoding by applying slow-down," *Proc. of IEEE Workshop on Signal Processing Systems*, pp. 19-24, Washington D. C., Oct. 2008.
43. B. Chen and X. Zhang, "Error correction for multilevel NAND flash memory using Reed-Solomon codes," *Proc. of IEEE Workshop on Signal Processing Systems*, pp. 94-99, Washington D. C., Oct. 2008.
44. Z. Cui, Z. Wang, X. Zhang and Q. Jia, "Hardware efficient LDPC decoding for magnetic recording," *Proc. of IEEE International Magnetics Conference,* Madrid, Spain, May 2008.
45. J. Zhu, X. Zhang and Z. Wang, "Novel interpolation architecture for low-complexity Chase soft-decision decoding of Reed-Solomon codes," *Proc. of IEEE International Symposium on Circuits and Systems,* pp. 3078-3081, Seattle, WA, May 2008.
46. B. Chen and X. Zhang, "FPGA implementation of a factorization processor for soft-decision Reed-Solomon decoding," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 944-947, Seattle, WA, May 2008.
47. J. Zhu and X. Zhang, "Efficient interpolation architecture for soft-decision Reed-Solomon decoding," *IEEE Workshop on Signal Processing Systems,* pp. 663-668, Shanghai, China, Oct. 2007.
48. X. Zhang and J. Zhu, "Low-complexity interpolation architecture for soft-decision Reed-Solomon decoding," *Proc. of IEEE International Symposium on Circuits and Systems*, pp. 1413-1416, New Orleans, LA, May 2007.
49. X. Zhang, "High-speed factorization architecture for soft-decision Reed-Solomon decoding," *Proc. of IEEE International Conference on Computer Design*, pp. 370-375, San Jose, CA, Oct. 2006.
50. X. Zhang, "Partial parallel factorization in soft-decision Reed-Solomon decoding," *Proc. of ACM Great Lakes Symposium on VLSI*, pp. 272-277, Philadelphia, PA, Apr. 2006.

51. X. Zhang and K. K. Parhi, "An efficient 21.56 Gbps AES implementation on FPGA," *Proc. of Asilomar Conference on Signals, Systems, and Computers*, pp. 465-470, Pacific Grove, CA, Nov. 2004.
52. X. Zhang and K. K. Parhi, "Fast factorization architecture in soft-decision Reed-Solomon decoding," *Proc. of IEEE Workshop on Signal Processing Systems*, pp. 101-106, Austin, TX, Oct. 2004.
53. X. Zhang and K. K. Parhi, "High-speed architectures for parallel long BCH encoders," *Proc. of ACM Great Lakes Symposium on VLSI*, pp. 1-6, Boston, MA, Apr. 2004.

Invited Conference Papers

1. X. Zhang, "Efficient nested key equation solver architectures for generalized Integrated interleaved codes," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2020.
2. X. Zhang, "Interpolation-based Chase BCH decoder," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2014.
3. X. Zhang, R. Shi and J. Ritcey, "Reducing the latency of Lee-O'Sullivan interpolation through modified initialization," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2013.
4. X. Zhang, R. Shi and J. Ritcey, "On the implementation of modified fuzzy vault for biometric encryption," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2012.
5. X. Zhang and Y. Zheng, "Efficient codeword recovery architecture for low-complexity Chase Reed-Solomon decoding," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2011.
6. X. Zhang and J. Zhu, "Hardware complexities of algebraic soft-decision Reed-Solomon decoders and comparisons," *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2010.
7. X. Zhang, "High-speed VLSI architecture for low-complexity Chase soft-decision Reed-Solomon decoding", *Proc. of Information Theory and Applications Workshop*, San Diego, CA, Feb. 2009.
8. X. Zhang and J. Zhu, "Efficient VLSI architecture for soft-decision Reed-Solomon decoding," *Proc. of 13th NASA Symposium on VLSI,* Post Falls, ID, Jun. 2007.

Conference Presentations

1. X. Zhang and Z. Xie, "Efficient architectures for generalized integrated interleaved decoder," IEEE International Symposium on Circuits and Systems, Seville, Spain, May 2020.
2. X. Zhang, "Improving the locality of generalized integrated interleaved codes," Flash Memory Summit, San Jose, CA, Aug. 2019.
3. X. Zhang, "A low-power parallel architecture for linear feedback shift registers," IEEE International Symposium on Circuits and Systems, Sapporo, Japan, May 2019.

4. X. Zhang, "Encoder and decoder for three-layer generalized integrated interleaved codes," Information Theory and Applications Workshop, San Diego, CA, Feb. 2019.
5. X. Zhang, "On the construction of composite finite field for hardware obfuscation," The Ohio State University Cybersecurity Days, Oct. 2018.
6. X. Zhang, "Modified generalized integrated interleaved codes for local erasure recovery," Non-Volatile Memories Workshop, San Diego, CA, Mar. 2018.
7. X. Zhang, "Improving the locality of generalized integrated interleaved codes," Information Theory and Applications Workshop, San Diego, CA, Feb. 2018.
8. X. Zhang and S. Sprouse, "A flexible and low-complexity local erasure recovery scheme," Flash Memory Summit, San Jose, CA, Aug. 2017.
9. X. Zhang, "Low-complexity transformed encoder architectures for quasi-cyclic non-binary LDPC codes over subfields," IEEE International Symposium on Circuits and Systems, Maryland, MA, May 2017.
10. X. Zhang, S. Sprouse, and I. Ilani, "A flexible and low-complexity local erasure recovery scheme," Non-Volatile Memories Workshop, San Diego, CA, Mar. 2017.
11. X. Zhang, I. Alrod, and S. Alterman, "On the application of non-binary LDPC codes to Flash memories and their hardware complexities," Non-Volatile Memories Workshop, San Diego, CA, Mar. 2016.
12. X. Zhang, S. Sprouse, and I. Ilani, "A flexible and low-complexity local erasure recovery scheme," International SanDisk Technology Conference, CA, Mar. 2016.
13. X. Zhang, I. Alrod, and S. Alterman, "On the application of non-binary LDPC codes to Flash memories and their hardware complexities," International SanDisk Technology Conference, CA, Mar. 2016.
14. X. Zhang, "VLSI architectures for non-binary LDPC decoder," Flash Memory Summit, San Jose, CA, Aug. 2015.
15. X. Zhang, "VLSI architecture design of XTS-AES for data storage," Flash Memory Summit, San Jose, CA, Aug. 2014.
16. X. Zhang, "Low-energy and low-latency error-correction for phase change memory", Non-Volatile Memories Workshop, San Diego, CA, Mar. 2013.
17. X. Zhang, "Error correction for multilevel NAND Flash memory using Reed-Solomon codes", Non-Volatile Memories Workshop, San Diego, CA, Mar. 2010.
18. X. Zhang, "VLSI architecture design for algebraic soft-decision Reed-Solomon decoding," Information Theory and Applications Workshop, San Diego, CA, Feb. 2008.

Patents

1. P. Mehra and X. Zhang, "Non-volatile storage system with application-aware error-correcting codes," Application # 20180358989, filed Sep. 2017.
2. X. Zhang and M. Hassner, "Systems, methods and devices for encoding and decoding data using multi-layer integrated interleaved codes," U. S. patent 10,256,843, Apr. 2019.

3. N. N. Yang, S. Sprouse, P. Reusswig, T. -C. Kuo, and X. Zhang, "Erasure correcting coding using temporary erasure data," U. S. patent 10,218,789, Feb. 2019.
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5. X. Zhang, et. al., "Column-layered message-passing LDPC decoder" U.S. patent 10,110,249, Oct. 2018.
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7. X. Zhang, Y. Ryabinin and E. Sharon, "On-the-fly syndrome and syndrome weight computation architecture for LDPC decoding," U.S. patent 9,768,807, Sep. 2017.
8. X. Zhang, "Interleaved layered decoder for low-density parity check codes," U.S. patent 9,748,973, Aug. 2017.
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10. X. Zhang and Y. Tai, "High-speed multi-block-row layered decoder for low density parity check (LDPC) codes," U.S. patent 9,602,141, Mar. 2017.
11. X. Zhang, "Modified trellis-based min-max decoder for non-binary low-density parity-check error-correcting codes," U.S. patent 9,503,125, Nov. 2016.
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14. J. Jiang, T. Tian, R. Krishnamoorthi and X. Zhang "Parity check matrix optimization and selection for iterative decoding," U.S. patent 8,443,255, May 2013.

INVITED PRESENTATIONS & TUTORIALS

1. "VLSI Architectures for Reed-Solomon Codes: Classic, Nested, Coupled, and Beyond," invited overview lecture, IEEE International Symposium on Circuits and Systems, virtual, Oct. 2020.
2. "Efficient architectures for error/erasure correcting codes," Kioxia Memory Corporation, Tokyo, Japan, May 2019
3. "Error-correcting codes for hyper-speed distributed storage: from theory to practice," University of California, Irvine, Apr. 2019.
4. Co-presenter for tutorial "Error-correcting decoder design for next-generation memories: from theory to practice," IEEE International Symposium on Circuits and Systems, Florence, Italy, May 2018.

5. "Error correcting codes: from hyper-scale distributed storage to security," University of Minnesota, Minneapolis, MN, Mar. 2018.
6. "Error correcting codes: from hyper-scale distributed storage to security," Nanjing University, Nanjing, China, Dec. 2017.
7. "Error correcting codes: from hyper-scale distributed storage to security," Fudan University, Shanghai, China, Dec. 2017.
8. "VLSI architecture design for algebraic soft-decision Reed-Solomon decoding," Ajou University, Seoul, Korea, May 2012.
9. "VLSI architecture design for algebraic soft-decision Reed-Solomon decoding," International Workshop on Coding and Cryptology, Qingdao, China, May 2011.
10. "Reduced-complexity decoder architecture for non-binary LDPC codes," University of Minnesota, Minneapolis, MN, Jun. 2010.
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