Hironori Uchikawa

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Summary

Hironori Uchikawa was born in Kanagawa, Japan in 1978. He received the B.E. and M.E. degrees in electrical engineering from Yokohama National University in 2001 and 2003 respectively. He received the Ph.D. degree in electrical engineering from Tokyo Institute of Technology in 2012. In 2003, he joined the Research and Development Center at Toshiba Corp. where he was engaged in research on MIMO-OFDM systems, especially for the IEEE 802.11n standard. Also, he developed error-correcting codes, especially low-density parity check (LDPC) codes, for NAND flash memory systems. Since 2013, he had been a Visiting Scholar in the Center for Memory Recording Research (CMRR) at University of California, San Diego and engaged in research on coding for distributed storage systems and flash memories. He also developed an FPGA-based platform for experiments of flash memories at the CMRR. He is currently a Senior Specialist in the System Technology Research and Development Center at Kioxia Corporation (formerly known as Toshiba Memory). His research interests include coding theory, information theory, communication theory and their applications to storage systems. He has authored and co-authored 28 international journal papers and conference papers, and he holds 44 U.S. patents. Dr. Uchikawa is a Senior Member of both the IEEE and the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan. He received the 2008 Young Researcher's Award of the IEICE.

Education

March 2012	PhD in Engineering, Tokyo Institute of Technology, Japan.
March 2003	M.E., Yokohama National University, Japan.
March 2001	B.E., Yokohama National University, Japan.

Honor

2008	Young Researcher's Award of the Institute of Electronics, Information and Communication Engineers (IEICE).

Professional Experience

2012–today **Senior Specialist at Kioxia Corporation (formerly known as Toshiba Memory).**
leads projects of ECC development for flash memory products in the System Technology Research and Development Center.

- Hardware-efficient LDPC code design and low-complexity iterative decoding algorithms.
- Algorithm design for low-complexity algebraic error-correcting codes.
- Characterization and modeling of flash memories.
- Reliability estimation of flash memories.

2015, 2017, and 2019 **Part-time Lecturer at Chiba University.**

2013–2014 **Visiting Scholar at UC San Diego.**
investigated protograph-based LDPC code design and published a conference paper at the ISIT2014 and developed an FPGA-based platform for experiments of flash memories.

2003–2012 **Research Scientist at Toshiba Corporation.**
worked at Wireless System Laboratory, Corporate Research and Development Center.

- Apr. 2006 - Sept. 2012: Research and development of error correcting codes for non-volatile memory systems.
- Apr. 2004 - Mar. 2006: Research and development of MIMO-OFDM systems for the IEEE 802.11n standard. Frame synchronization for multi antenna OFDM systems.
- Dec. 2003 - Mar. 2004: Software engineering training at CDAC-ACTS in Pune, India.
- Jul. 2003 - Nov. 2003: Development of adaptive array antenna for wireless LAN system. Evaluation of auto gain control algorithms for multi antenna OFDM system.

Professional Activities

- Reviewer for IEICE and IEEE journals, and numerous IEEE conferences.
- TPC member for NVMW2018–2013, ICNC2013, and Workshop on Coding for Flash Memories 2012.
- Vice-Chair from Industry of Data Storage Technical Committee in IEEE ComSoc 2018–2020.
- General Secretary of the symposium committee for the International Symposium on Information Theory and Its Applications (ISITA) 2020.
- Guest Editor of special issue on Information Theory and Its Applications 2013 of IEICE Transactions.
- Senior Member of both the IEEE and the IEICE.

Publications

Peer-reviewed Articles

1. P. Huang, E. Yaakobi, H. Uchikawa, and P. H. Siegel, "Binary linear locally repairable codes," *IEEE Transactions on Information Theory*, vol. 62, pp. 6268–6283, Nov. 2016

2. V. Taranalli, H. Uchikawa, and P. H. Siegel, "On the capacity of the beta-binomial channel model for multi-level cell flash memories," *IEEE Journal on Selected Areas in Communications*, vol. 34, pp. 2312–2324, Sept. 2016

3. V. Taranalli, H. Uchikawa, and P. H. Siegel, "Channel models for multi-level cell flash memories based on empirical error analysis," *IEEE Transactions on Communications*, vol. 64, pp. 3169–3181, Aug. 2016

4. H. Goto and H. Uchikawa, "Soft-decision decoder for quantum erasure and probabilistic-gate error models," *Phys. Rev. A*, vol. 89, p. 022322, Feb. 2014

5. H. Goto and H. Uchikawa, "Fault-tolerant quantum computation with a soft-decision decoder for error correction and detection by teleportation," *Scientific Reports*, vol. 3, no. 2044, 2013

6. H. Uchikawa, K. Kasai, and K. Sakaniwa, "Spatially coupled protograph-based LDPC codes for decode-and-forward in erasure relay channel," *IEICE Trans. Fundamentals*, vol. E94-A, no. 11, pp. 2127–2134, 2011

7. H. Uchikawa, K. Kasai, and K. Sakaniwa, "Design and performance of rate-compatible non-binary ldpc convolutional codes," *IEICE Trans. Fundamentals*, vol. E94-A, no. 11, pp. 2135–2143, 2011

8. K. Harada, H. Obata, H. Uchikawa, K. Yoshida, and Y. Sakai, "Optimum soft-output of autoregressive detector for offtrack interference in LDPC-coded perpendicular magnetic recording," *IEICE Trans. Fundamentals*, vol. E93-A, pp. 1966–1975, Nov. 2010

9. H. Uchikawa and K. Harada, "Complexity-reducing algorithm for serial scheduled min-sum decoding of LDPC codes," *IEICE Trans. Fundamentals*, vol. E92-A, pp. 2411–2417, Oct. 2009

10. H. Uchikawa, K. Umebayashi, and R. Kohno, "Secure download system based on software defined radio composed of FPGAs," *IEICE Trans. Communications*, vol. E85-B, pp. 2601–2609, Dec. 2002

Peer-reviewed Conferences

1. N. Kokubun, D. Watanabe, H. Uchikawa, and P. H. Siegel, "Approximated em algorithms for estimation of unknown coded discrete memoryless channels," in *Proc. 2020 IEEE GLOBECOM*, Dec. 2020. Taiwan

2. N. Kokubun, A. Yamaga, H. Uchikawa, and D. Watanabe, "Circuit-size reduction for parallel chien search using minimal polynomial degree reduction," in *Proc. Int. Symp. on Circuits and Systems (ISCAS2019)*, May 2019. Sapporo, Japan

3. Y. Kumano, Y. Sakamaki, and H. Uchikawa, "Complete multipartite graph codes," in *Proc. Int. Symp. on Inf. Theory and its Applications (ISITA2018)*, pp. 237–241, Oct. 2018. Singapore

4. N. Kokubun and H. Uchikawa, "Integrated parallel interleaved concatenation for lowering error floors of LDPC codes," in *Proc. 2016 IEEE Int. Symp. Inf. Theory (ISIT)*, pp. 3013–3017, Aug. 2016. Barcelona, Spain

5. P. Huang, E. Yaakobi, H. Uchikawa, and P. H. Siegel, "Linear locally repairable codes with availability," in *Proc. 2015 IEEE Int. Symp. Inf. Theory (ISIT)*, pp. 1871–1875, July 2015. Hong Kong, China

6. V. Taranalli, H. Uchikawa, and P. H. Siegel, "Error analysis and inter-cell interference mitigation in multi-level cell flash memories," in *Proc. 2015 IEEE Int. Conf. Commun.(ICC)*, pp. 1868–1873, June 2015. London, UK

7. P. Huang, E. Yaakobi, H. Uchikawa, and P. H. Siegel, "Cyclic linear binary locally repairable codes," in *Proc. 2015 IEEE Information Theory Workshop (ITW)*, pp. 1–5, Apr. 2015. Jerusalem, Israel

8. H. Uchikawa, "Design of non-precoded protograph-based ldpc codes," in *Proc. 2014 IEEE Int. Symp. Inf. Theory (ISIT)*, pp. 2779–2783, July 2014. Honolulu, USA

9. H. Uchikawa, B. Kurkoski, K. Kasai, and K. Sakaniwa, "Iterative encoding with gauss-seidel method for spatially-coupled low-density lattice codes," in *Proc. 2012 IEEE Int. Symp. Inf. Theory (ISIT)*, pp. 1747–1751, Aug. 2012. Boston, USA

10. H. Uchikawa, B. Kurkoski, K. Kasai, and K. Sakaniwa, "Threshold improvement of low-density lattice codes via spatial coupling," in *Proc. 2012 IEEE Int. Conf. on Computing, Networking and Communications (ICNC)*, pp. 1036–1040, Feb. 2012. Hawaii, USA

11. H. Uchikawa, K. Kasai, and K. Sakaniwa, "Spatially coupled protograph-based LDPC codes for decode-and-forward in erasure relay channel," in *Proc. 2011 IEEE Int. Symp. Inf. Theory (ISIT)*, pp. 1479–1483, Aug. 2011. Saint-Petersburg, Russia

12. H. Uchikawa, K. Kasai, and K. Sakaniwa, "Terminated LDPC convolutional codes over gf(2^p)," in *Proc. 48th Annual Allerton Conf. on Commun., Control, and Computing*, pp. 195–200, Oct. 2010. Illinois, USA

13. H. Uchikawa, K. Harada, and Y. Tanabe, "Reduced-complexity serial min-sum decoding," in *Proc. 5th Int. Symp. on Turbo Codes and Related Topics*, pp. 145–150, Sept. 2008

14. K. Harada and H. Uchikawa, "Reliable soft-output of autoregressive ml detector for perpendicular magnetic recording with intertrack interference," in *Proc. Int. Symp. on Inf. Theory and its Applications (ISITA2008)*, pp. 1–6, Dec. 2008. Auckland, New Zealand

15. H. Uchikawa, K. Harada, and Y. Tanabe, "Ordered shuffled belief propagation decoding for irregular LDPC codes," in *Proc. The 10th International Symposium on Wireless Personal Multimedia Comunications (WPMC)*, no. Tu-3C-3, pp. 348–352, 2007

16. K. Okuike, H. Uchikawa, K. Ikemoto, K. Umebayashi, and R. Kohno, "On-board automatic certificating system (ACS) for software defined radio," in *Proc. 2002 SDR Technical Conferece*, pp. 103–106, Nov. 2002. San Diego, USA

17. H. Uchikawa, K. Umebayashi, and R. Kohno, "Secure download system based on software defined radio composed of FPGAs," vol. 1, pp. 437–441, Sept. 2002. Lisbon, Portugal

18. H. Uchikawa, K. Ikemoto, K. MIZUTANI, K. Umebayashi, and R. Kohno, "Adaptive security levels control method based on software defined radio," in *Proc. The Fourth International Symposium on Wireless Personal Multimedia Comunications (WPMC)*, pp. 1503–1508, Sept. 2001. Aalborg, Denmark

Book

1. H. Uchikawa, "Error correcting codes based on probabilistic decoding and sparse matrices," *A Mathematical Approach to Research Problems of Science and Technology*, pp. 495–504, 2014